## **ORIGINALLY SUBMITTED INFORMAL DRAWINGS**

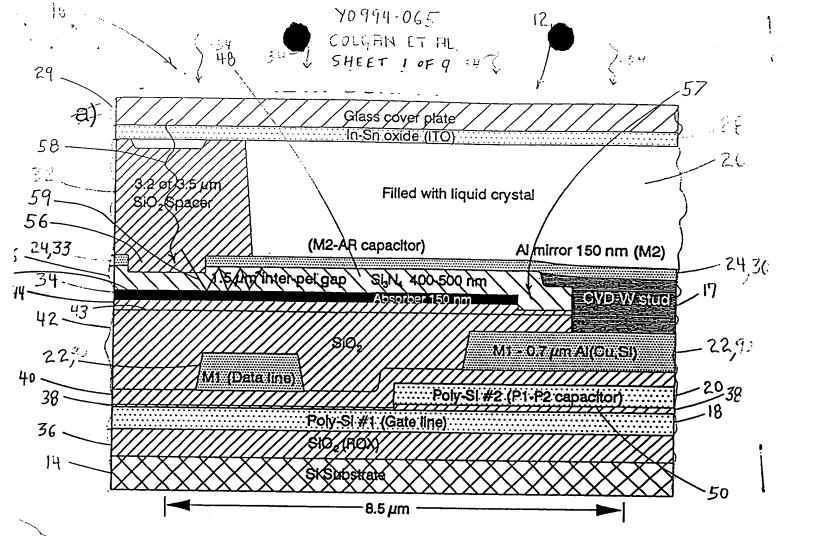
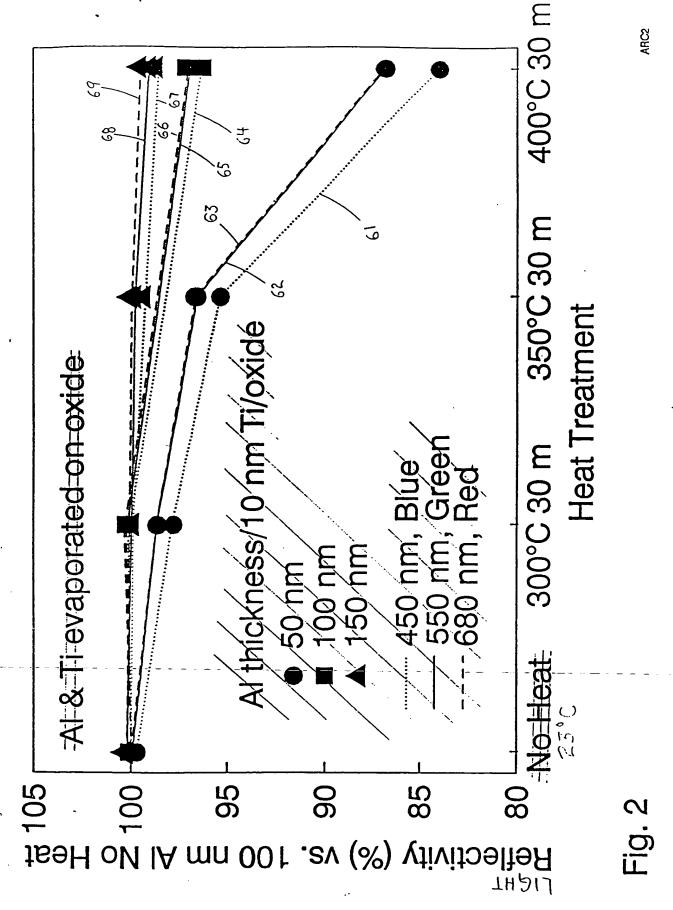
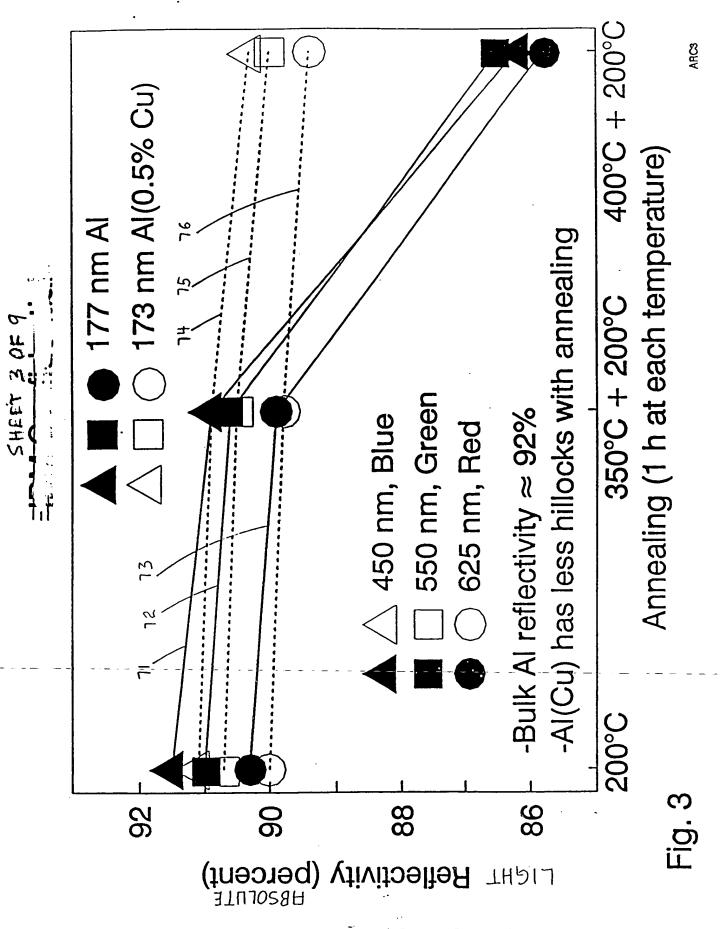


FIG 1

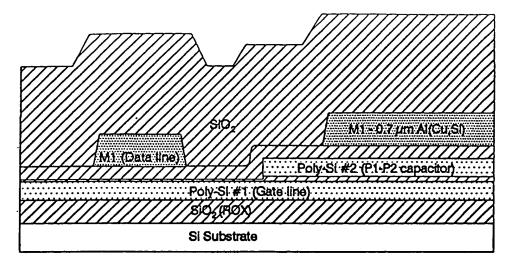




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a) Liftoff 0.7  $\mu$ m Al(Cu,Si) M1. Deposit thick oxide.

F19 5

M1 (Data line)  M2 (Poly-Si #2 (P1-P2 capacitor)
Poly-Si #1 (Gate line)
\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
Si Substrate

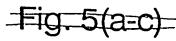
b) CMP oxide leaving 500 nm on highest M1 point.Deposit 200 nm oxide.

F16 6

Absorber 150 pm
M1 - 0.7 μm Al(Cu;Si)
M1:(Deta line)
Poly-Si.#2 (P1-P2 capacitor)
Poly-Si #1 (Gate line)
\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
Si Substrate

c) Deposit 10 nm TV 100 nm AV 50 nm TiN, pattern with AR mask.
Deposit 400-500 nm nitride.

FIG 7



# -----96

Sign 400-500 hm

| Gyo-yy-siers|
| M1 - 0.7 \( \text{pm Al(Cu(Si))} \)
| M1. (Data line) | Poly-Si #2 (P1-P2 capacitor) |
| Poly-Si #1 (Gate line) |
Sign	Poly-Si #2 (P1-P2 capacitor)
Sign	Poly-Si #1 (Gate line)
Sign	Poly-Si #2 (P1-P2 capacitor)
Sign	Poly-Si #1 (Gate line)
Sign	Poly-Si #2 (P1-P2 capacitor)
Sign	Poly-Si #1 (Gate line)
Sign	

d) Pattern with V1 mask.
 Deposit liner & CVD-W.
 W Chem-mech polish.

FIG 8

Al mirror 150 nm (M2)

1,5 mm inter-pet gap Si,W, 400-500 nm
Absorber 150 nm
Absorber 150 nm
Absorber 150 nm
Absorber 150 nm
Al mirror 150 nm (M2)

Absorber 150 nm
Absorber 150 nm
Absorber 150 nm
Absorber 150 nm
Al -0.7 mm Al(Ctr;Sl)

M1::(Data:line)

Poly-Si #2 (P1-P2 capacitor)

Si Substrate

e) Deposit 10 nm Ti/ 150 nm Al, pattern with M2 mask.

(M2-AR capacitor)

Al mirror 150 nm (M2)

1.5 2m Intel pelicals Sign 400-508 nm

1.3301-33150 nm

M1: (Data line)

Poly-Si #1 (Gate line)

Si Substrate

 Deposit 2.2 or 3 μm oxide, pattern with SP mask. Open up M1 pads with TV mask.

Fig. 5(d=f)

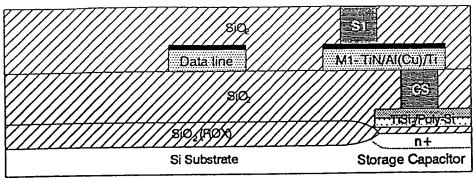
FIG 10

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ARC5B

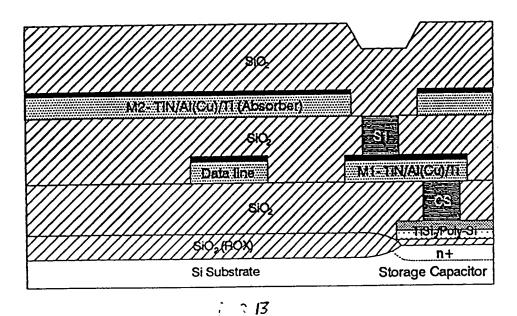
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a) 15 µm

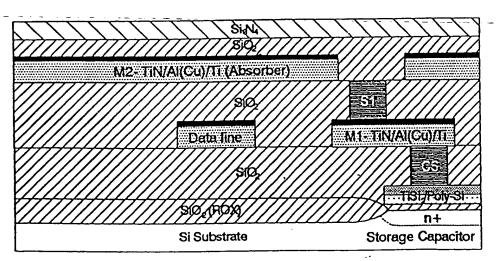


a) Use standard CMOS 4 process to S1.

F 6 12



 b) Pattern POR M2 as Absorber layer. POR oxide deposition.



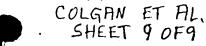
on highest M2 point.

Deposit 300 nm nitride.

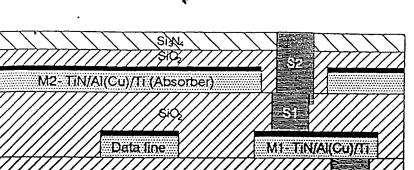
Fig. 8(a-c)

1:514

ARC8A



Storage Capacitor



d) Pattern with S2 mask. Deposit liner & CVD-W. W Chem-mech polish. Stacked S1&S2 to connect M1 & M3.

FIG 15

Si Substrate

M3- 150 nm Al or Al(Cu)/10 nm Ti (Mirror)

Signal

M2:TIN/Al(Cu)/TI (Absorber)

Data:line

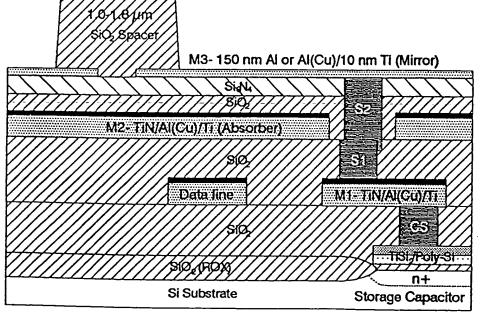
M1:TIN/Al(Cu)/TI

Signal

Sign

e) Deposit 10 nm Ti/ 150 nm Al, pattern with M3 mask.

F15 16



 Deposit 1.0 or 1.8 μm oxide, pattern with SP mask. Open up M2 pads with TV mask.

Fig. 8(d=f)\_ Fig. 17

ARC6B